**COMPUTER ORGANIZATION AND ARCHITECTURE (PC404EC)**

***QUESTION BANK (2021-2022)***

**B.E. ECE IV SEM (AMC) SECTION A**

**UNIT I [Data representation & Computer Arithmetic]**

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**UNIT II [Basic Computer Organization & Design]**

**Short Type Questions**

1. Perform the arithmetic operation (-52) - (-13) in binary using signed 2’s complement representation for negative numbers.
2. Represent the number (+ 37.5) in IEEE 754 single precision format.
3. What is normalization and alignment in floating point arithmetic?
4. Differentiate between restoring and non-restoring division algorithm.
5. Show the hardware for signed 2’s complement addition and subtraction.
6. Show the hardware for implementing Booth’s algorithm.
7. What is stored program organization?
8. Write the instruction formats for memory reference and register reference instructions of a basic computer.
9. What is the difference between a direct and an indirect address instruction? Illustrate with an example.
10. Explain the purpose of the following registers in basic computer:

(i) PC (ii) DR (iii) IR

1. Compare Hardwired and Microprogrammed Control Organization.
2. What are the sub phases in an Instruction cycle of a basic computer?

14. Define the following terms: i) Micro operation ii) Micro instruction

iii) Micro program.

1. Hardwired Control is faster than micro-programmed control unit. Justify

this statement.

15. Draw the microinstruction format and specify each field.

**Essay Type Questions**

1. Explain about the IEEE 754 Standard floating point representation formats with suitable examples.
2. Using Booth’s algorithm, show the step-by-step multiplication process for the following example (+8) × (-9). Assume 5-bit registers that hold signed numbers.
3. Explain the process of floating point number multiplication with a neat flow chart.
4. Show the contents of registers E, A, Q and SC during the process of division of 10100011 by 1011. (Use a dividend of eight bits).
5. Draw the flow chart for a sign magnitude integer addition and subtraction algorithm and explain.
6. With a neat diagram of a common bus system, show how to execute the micro operation

AC AC + DR

1. Draw the block diagram of a control unit of a basic computer and explain.
2. Explain the various phases of an Instruction cycle with a flow chart.
3. List the control functions and micro operations needed for the execution of the following memory reference instructions:

(i)BUN (ii) BSA (iii) ISZ (iv) LDA

1. Write the micro operations needed for the fetch and decode phases of an instruction cycle and explain.
2. Explain the input-output configuration of a Basic computer and list any four I/O instructions with their control functions and micro operations.
3. Draw and explain the flow chart for an interrupt cycle. Write the sequence of micro operations for the same.
4. Show how a 9-bit micro operation field in a micro instruction can be divided into subfields to specify 46 micro operations. How many micro operations can be specified in one micro instruction?
5. What is the purpose of microprogram sequencer? Explain with block diagram, how the sequencer present addresses to control memory.

**UNIT III [Central Processing Unit]**

**Short Type Questions**

1. What the advantages are of stack organized computer?
2. Write the need for different addressing modes.
3. Write the differences between RISC and CISC processors.
4. Determine the number of clock cycles that it takes to process 200 tasks in a six segment pipeline.
5. Mention the different types of instruction formats.
6. What is a stack and what is its role in the operation or execution of computer instructions?
7. Discuss various types of CPU organizations.
8. Write the features of a RISC processor.
9. A non-pipeline takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?
10. What is meant by pipeline hazard?
11. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.
12. What are the different addressing modes of a basic computer?
13. What is vector processing?

**Essay Type Questions**

1. Explain instruction formats for various types of computer organizations as single accumulator, general register and stack.
2. Draw the organization of a 64-word register stack and explain its PUSH and POP operations using register microoperations.
3. Explain various types of interrupts in brief.
4. What is the need for addressing mode? Explain various addressing modes of general purpose computer.
5. Explain data manipulation operations of a basic computer.
6. How is vector processing is different from Array processing. Give their application areas.
7. Explain pipeline conflicts and discuss their remedies.
8. Compare CISC and RISC Architectures.
9. Classify the instructions based on the fields of a instruction format.
10. Draw a flow chart for a six stage CPU instruction pipeline and explain.
11. An instruction is stored at location 300H with its address field at 301H. The address field has the value 400H. A processor register R1 contains the number 200H. Evaluate the effective address if the addressing mode of the instruction is

i) direct ii) Immediate iii) Relative iv) Register indirect

v) Index with R1 as the Index register.

**UNIT IV**

**Input-Output Organization**

**Short Type Questions**

1. List the advantages of memory-mapped I/O techniques.
2. Why does DMA have a priority over the CPU when both request a memory transfer?
3. Give at least six status conditions for setting of individual bits in the status register of an asynchronous communication interface.
4. What is the need for an I/O interface?
5. Differentiate between Synchronous and Asynchronous data transfer.
6. Mention the ways that computer buses can be used to communicate with memory and I/O.
7. Draw the flowchart for destination initiated transfer using handshaking.

**Essay Type Questions**

1. Explain Daisy-chain interrupt priority and draw the logic circuit for one

stage of daisy-chain priority arrangement.

1. Design a parallel priority interrupt hardware for a system with four interrupt sources.
2. Explain the functions of a typical 8-bit parallel interface in detail.
3. Write the differences between memory-mapped I/O and I/O mapped I/O.
4. Draw and explain the block diagram of an asynchronous communication interface.
5. Describe in detail how data is transferred using DMA. Draw the necessary diagrams to support your explanation.
6. Describe CPU-IOP communication process using a flow chart.

**UNIT V**

**Memory Organization**

**Short Type Questions**

1. How many 256 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
2. What is meant by “locality of reference” and how does it help in faster execution of programs?
3. Differentiate between Temporal locality and spatial locality.
4. What do you mean by page fault? Which hardware is responsible for detecting the page fault?
5. Explain the terms Tag, Index and Block in relation to cache memory.
6. Distinguish between RAM and CAM (Associative memory).
7. What is address space and memory space in virtual memory system?
8. What are the basic components of a memory management unit?

**Essay Type Questions**

1. What do you mean by memory hierarchy? Describe it in detail.
2. What is cache memory? How its performance can be increased? Discuss.
3. A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K × 32.
4. Formulate all pertinent information required to construct the cache memory.
5. What is the size of the cache memory?
6. A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
7. How many bits are there in the tag, index, block, and word fields of the address format?
8. How many bits are there in each word of the cache, and how are they divided into functions? Include a valid bit.
9. How many blocks can the cache accommodate?
10. Why page-table is required in virtual memory system? Explain different ways of organizing a page table.
11. Explain in detail about virtual memory address translation.
12. Derive the Match logic for one word of associative memory and explain.
13. Describe the segmented-page mapping process in a typical memory management unit using suitable diagrams.
14. An address space is specified by 24 bits and the corresponding memory space by 16 bits.
15. How many words are there in the address space?
16. How many words are there in the memory space?
17. If a page consists of 2K words, how many pages and blocks are there in the system?

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